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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/829,146	04/21/2004	Nobuaki Hashimoto	81751.0071	81751.0071 5088	
26021	7590 01/27/2005		EXAMINER		
HOGAN & HARTSON L.L.P.			OWENS, DOUGLAS W		
500 S. GRAND AVENUE SUITE 1900			ART UNIT	PAPER NUMBER	
	LES, CA 90071-2611		2811	2811	
			DATE MAILED: 01/27/2009	DATE MAILED: 01/27/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)		
Office A stiers Cours		10/829,146	HASHIMOTO, NOBUAKI		
Office Acti	on Summary	Examiner	Art Unit		
		Douglas W. Owens	2811		
The MAILING D. Period for Reply	ATE of this communication app	ears on the cover sheet with the c	correspondence address		
THE MAILING DATE (- Extensions of time may be averafter SIX (6) MONTHS from the lift the period for reply specifiering the lift NO period for reply is specifiering to reply within the set	OF THIS COMMUNICATION. railable under the provisions of 37 CFR 1.13 he mailing date of this communication. d above is less than thirty (30) days, a reply field above, the maximum statutory period w or extended period for reply will, by statute, ice later than three months after the mailing	IS SET TO EXPIRE 3 MONTH(36(a). In no event, however, may a reply be tin within the statutory minimum of thirty (30) day rill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE date of this communication, even if timely filed	nely filed s will be considered timely. the mailing date of this communication. 10 (35 U.S.C. § 133).		
Status					
1) Responsive to co	ommunication(s) filed on				
2a) ☐ This action is FI	· · ·				
, -	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.				
Disposition of Claims		•			
4a) Of the above 5) ☐ Claim(s) i 6) ☑ Claim(s) <u>1-6</u> is/a 7) ☐ Claim(s) i	re rejected.				
Application Papers					
9) The specification	is objected to by the Examine	r.			
10)⊠ The drawing(s) filed on <u>21 April 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.					
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
	•	on is required if the drawing(s) is ob aminer. Note the attached Office			
Priority under 35 U.S.C. §	§ 119				
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 					
Attachment(s) 1) Notice of References Cited	d (PTO-892)	4) 🔲 Interview Summary	(PTO-413)		
2) Notice of Draftsperson's P.	atent Drawing Review (PTO-948) tement(s) (PTO-1449 or PTO/SB/08)	Paper No(s)/Mail Di			

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DETAILED ACTION

Claim Objections

1. Claims 1 and 5 is objected to because of the following informalities: in line 5, -the-- or --an-- should be inserted between "with" and "inside". Claim 5 has the same
problem in line 7. Appropriate correction is required.

2. Claim 3 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The claim merely recites an intended use, with no further structural limitations.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 4. Claims 1 6 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,313,532 to Shimoishizaka et al.

Regarding claim 1, Shimoishizaka et al. teach an electronic device (Figs. 5 and 9, for example) comprising:

a semiconductor substrate (1) in which an integrated circuit is formed;

an insulating layer (20) which is formed on the semiconductor substrate and includes an elastically deformable section;

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an electrode (32) which is electrically connected with the inside of the semiconductor substrate and is formed on the elastically deformable section; and

a substrate (61) on which an interconnect pattern (62) is formed, the interconnect pattern facing the electrode and being electrically connected with the electrode,

wherein the elastically deformable section is elastically deformed in a manner to be depressed under the electrode, and presses the electrode against the interconnect pattern due to elasticity.

Regarding claim 2, Shimoishizaka et al. teach an electronic device, further comprising a bump (41) formed between the electrode and the interconnect pattern, the electrode being electrically connected with the interconnect pattern through the bump.

Regarding claim 3, Shimoishizaka et al. teach an electronic device, wherein the bump includes a nickel layer (Col. 9, lines 33 - 37).

Regarding claim 4, Shimoishizaka et al. teach an electronic instrument comprising the electronic device claimed above.

Regarding claim 5, Shimoishizaka et al. teach a method of manufacturing an electronic device, comprising:

mounting a semiconductor device on a substrate on which an interconnect pattern is formed (Fig. 9);

wherein the semiconductor device includes a semiconductor substrate (1) in which an integrated circuit is formed, an insulating layer (20) which is formed on the semiconductor substrate and includes an elastically deformable section, and an

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electrode (32) which is electrically connected with the inside of the semiconductor substrate and is formed on the elastically deformable section; and

wherein, in the mounting step, the semiconductor device and the substrate are disposed so that the electrode faces the interconnect pattern, and the elastically deformable section is elastically deformed in a manner to be depressed under the electrode.

Regarding claim 6, Shimoishizaka et al. teach a method of manufacturing an electronic device, wherein the semiconductor device further includes a bump (41) on the electrode; and

Wherein the elastically deformable section is elastically deformed through the bump.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

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Douglas W Owens

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Examiner Art Unit 2811